HDI Materials with Higher Tg

Dr. James Briguglio

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Technology Drivers for New HDI Material Properties and Processing Conditions

Agenda

- Current Material Properties & Processing Conditions
- Currently Available Products
- Multek Technology Roadmap
- Industry Trends - New Drivers
- Translated New Properties
- New Processing Conditions
- Proposed Formulation Plans
- Testing Criteria

Why Do We Need a Higher Tg Material?

- Lower Coefficient of Thermal Expansion
- Increased Robustness for Assembly and Rework Processes
- Higher Cure Temperatures for Non-Halogenated Laminates
- Higher Reflow Temperatures for Lead Free Finishes

Currently Available Products

- Resin Coated Coppers
- Dry Film
  - Photo-Imageable (DynaVia)
  - Laser Ablate (Vialux)
- Liquid
  - Photo-Imageable (Probelac 81)
  - Laser Ablate (Probelac 81)

Technology Roadmap: Multek - Irvine

	Manufacturing	Standard Products	Advanced Products	Emerging Products			
		1999	1999	1999+	2000	2001	2002
1	Drilling Aspect Ratio - Drilled Hole Size	10:1	11.5:1	12:1	14:1	15:1	16:1
2	Min. Drilled Hole Size (vias)	.010	.006	.004	.005	.004	.004
3	Min. Finished Hole Size (vias)	.008	.004	.002	.003	.002	.002
4	Min. Outer Layer Via Land Size	.022	.013	.009	.015	.012	.010
5	Min. Inner Layer Via Land Size	.020	.012	.008	.015	.012	.010
6	Min. Via Relief on Power/Ground Planes	.024	.020	.018	.021	.018	.018
7	Min. Blind/Buried Via Land Size	.018	.016	.010	.014	.012	.010
8	Min. Blind/Buried Via Hole Size (Drilled)	.010	.006	.004	.005	.004	.004
9	Min. Outer Layer Line Width	.005	.004	.003	.0015	.001	.001
10	Min. Inner Layer Line Width	.004	.003	.002	.0015	.001	.001
11	Min. Outer Layer Line to Line Spacing	.005	.004	.003	.0015	.001	.001
12	Min. Inner Layer Line to Line Spacing	.004	.003	.002	.001	.001	.001
13	Min. Line to Via Land Spacing	.005	.004	.003	.0015	.0015	.001
14	Layer to Layer Registration Tolerance	+/-0.004	.0035	.003	.003	.002	.002

Technology Roadmap: Multek - Irvine

	Manufacturing	Standard Products 1999	Advanced Products 1999	Emerging Products 1999+	2000	2001	2002
15	Min. Component Pitch	.019	.008	.005	.006	.005	.004
16	Max. Overall Board Thickness	.250	.500	1.080	1.080	1.080	1.080
17	Min. Dielectric Thickness	.0027	.0022	.002	.0017	.0015	.0012
18	PCB Edge to Conductor Solder	.015	.010	.010	.007	.006	.005
19	Clearance per Side	.0045	.0035	.0025	.0025	.002	.002
20	Line to SMT Minimum Space	.007	.006	.004	.0045	.0045	.004
21	Min. Base Copper Weights	.0007	.00035	.00035	.00017	.00009	.00009
22	Average Layer Count	14	18	24	20	20	24
23	Dimensions - FAB O.D.	18x24	22x34	22x34	22x34	22x36	22x38
24	Fabrication Radius	.031	.016	.010	.0120	.012	.010
25	Warpage (Design Dependant)	1%	0.7%	0.5%	0.5%	0.5%	0.5%
26	Tolerance-Plated Holes (Design Dependant)	+/- .003	+/- .002	+/- .002	+/- .002	+/- .0015	+/- .001
27	Impedance Tolerance	+/- 10%	+/- 7%	+/- 5%	+/- 5%	+/- 5%	+/- 5%

Technology Roadmap: Multek - Irvine

1	Min. Component Pitch	.019	.010	.005	.005	.003	.002
2	Type of Test Equipment	Universal	Probe	Probe	Probe	Humbird	Humbird

Surface Finishes

- **Tin/Lead (Fused or HASL)**
- **Nickel/Gold: Electroplated (soft and hard), electroless nickel/immersion gold**
- **Organic coatings**
- **100% Tin**
- **Selective finishes**

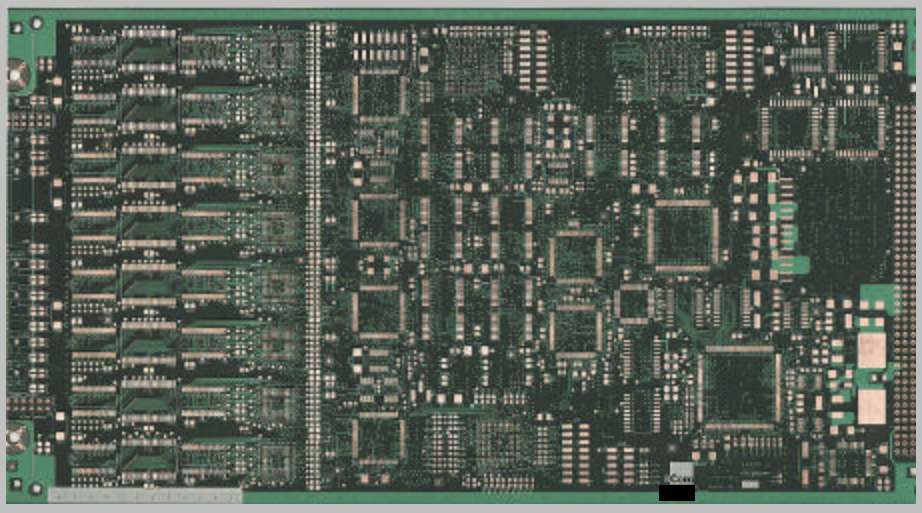
Material Types

- **Multifunctional FR-4**
- **Cynate Ester**
- **Polyimide**
- **BT**
- **Teflon**
- **Ohmega-Ply Resistors**
- **Buried Capacitors**
- **Low Dk, Low Df**

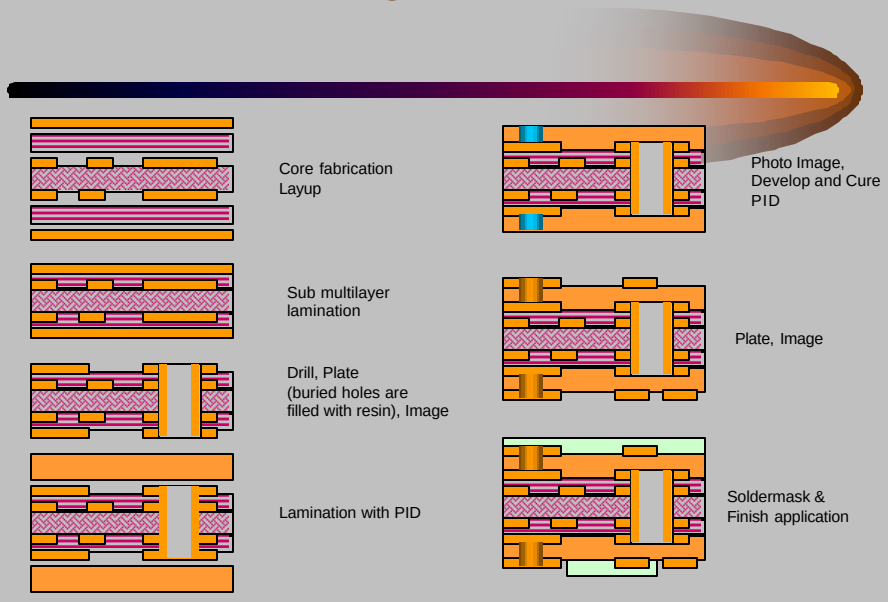
Current Material Properties

Material	**Epoxy Dry film, 2.5 mils Thick**	
Pencil Hardness	**8H**	
Solder Shock 270° C	**20 sec**	
Flammability	**UL 94 V-0**	
Dielectric Strength	**4000 V/mil**	
Dielectric Constant	**3.30 100 MHz**	**3.19 (1 GHz)**
Dielectric Loss	**$1.13e^{-2}$ 100 MHz**	**$1.10e^{-2}$ (1 GHz)**
Tg (DSC)	**118° C**	
CTE below Tg	**78 ppm**	
above Tg	**176 ppm**	
Decomposition Temperature	**340° C**	
Copper Adhesion	**1100 grams/cm (6.2 lbf/in)**	

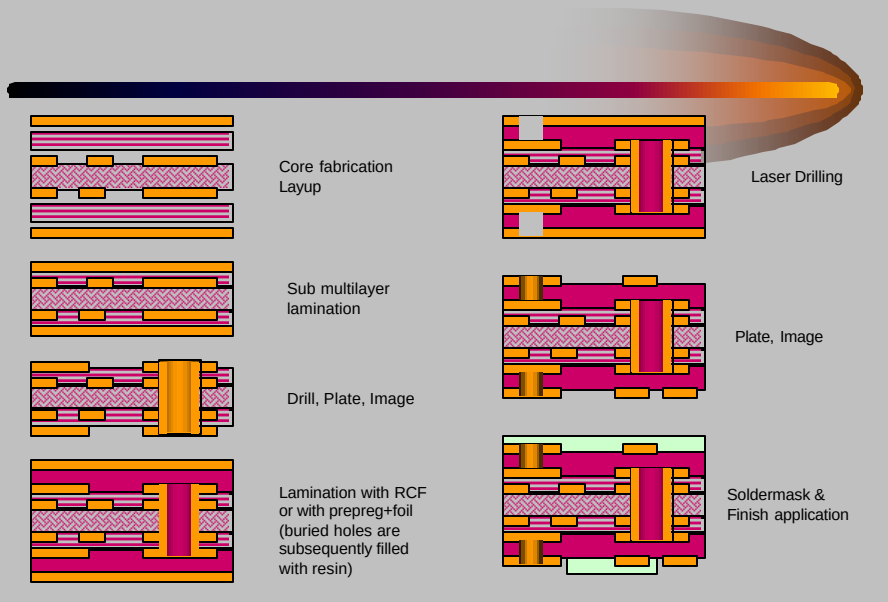
HDI 8s 2p, 1 build up layer each side



HDI Photo Image Dielectric Process



HDI Laser or Mechanical Drill Process



Industry Trends - New Drivers

- Smaller Holes & Larger Quantity
- Thinner Material to Maintain Aspect Ratio
- Improved Dielectric Performance
  - Lower Dk, Lower Loss Tangent
- Matched CTE
- Peel Strengths above 6.2 lbs
- Lower Moisture Absorption Properties
- Compatibility with non-halogenated laminates
- Tg above 180 C
- Compatible with Lead Free Finishes & Underfills

Translated Material Properties

Material	**Epoxy Based Dielectric**
Pencil Hardness	**9H**
Solder Shock 270° C	**Multiple Shocks**
IST Cycling	**Establish per IPC**
Flammability	**UL 94 V-0**
Dielectric Strength	**Above 4000 V/mil**
Frequency Requirement	**Up to 20 GHz**
Tg (DSC)	**180° C +**
CTE below Tg	**78 ppm**
above Tg	**176 ppm**
Decomposition Temperature	**340° C**
Copper Adhesion	**> 1100 grams/cm (6.2 lbf/in)**

Desired Processing Attributes

- Low Expose Dosage
  - Driven by cationic photoiniator which prefers an abundance of shorter wavelengths than provided by conventional and mercury arc lamps.
- Latent Image
  - Provides significant benefit for checking photovia registration and provides evidence of panel processing.
- Good Image Definition, Consistency of Photovia Shape
- Favorable Electrical Performance
  - Defined as resistance to electromigration in pressure cooker bias test.
- High Tg
  - Evidence of materials with lower Tg less robust in wire bond and repair applications.

Desired Processing Attributes

- No Squeeze Out at Lamination
- Strippable after Expose
- No Need for Adhesion Promotion on Underlying Copper
- Thickness Variation
  - Planarity deviations of < 5 microns over fineline circuitry.
- Developing Sensitivity
- Plated Copper to PID Adhesion
  - > 6.2 lbs

Desired Processing Attributes

- Shelf Life
  - Non-Refrigerated
- Surface Prep for Plating
  - Conventional Methods
- Good Hardness & Abrasion Resistance
- Low Cost
- Environmentally Friendly

Proposed Formulation Plans

- Epoxy Based Polymers
- Oligomers
- Monomers
- Curing Agents
- Fillers
- Additives
- Pigments

Testing Criteria

- IPC-600
- JEDEC
- Bellcore
- MilSpec
- IST to meet IPC Recommendations
- Instron Testing
- Pencil Hardness
- Solvent-Alkaline-Permanganate Resistance
- Imageability to 3 mil vias
- General Electrical Properties
- U.L. Approval
- Compatibility with Lead Free Finishes

Contributors

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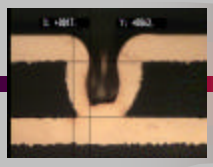
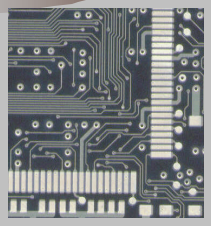
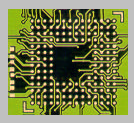
HDI Photo & Laser Drill Process



Micro Via
- experience since 1994
- volume manufacturing (6000 sqm/month)
High density interconnects
- buried vias / buried boards
- Micro BGA / CSP
- 3 mil lines / spaces on all layers
- electrical test capabilities
- registration capabilities
- 2 layers microvia available
- Stacked microvia available

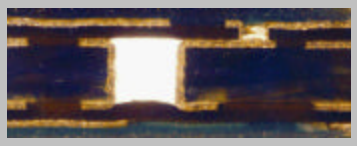




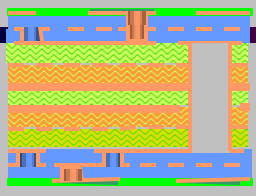
Lamination with
Resin Coated Foil

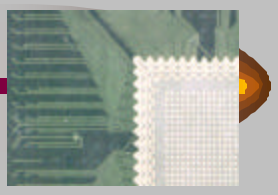
Copper Reduction

Copper and Dielectric
"Drilling"
with Nd-Yag Laser
(120 vias per sec)

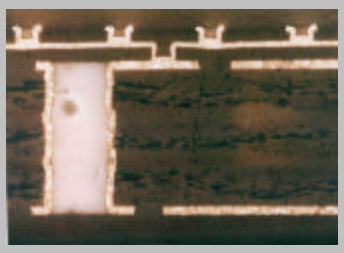


HDI Multi Layer Photo Process





- Prototype Capability installed



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